LJ64H052

SHARP

Features

- **Display size:** 26 cm [10.4″]
- **Display format:** 640 (W) × 480 (H) dots
- **Dot pitch:** 0.33 (W) × 0.33 (H) mm
- **Input signal level:** CMOS level
  (Compatible with Passive dot matrix LCD)
- **Drive method:** P-P symmetric drive
- **Structure:** Baseplate
- **Weight:** Approx. 680 g*
  *Including DC/DC converter

■ Absolute maximum ratings

(Ta=25 °C)

Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	V_L + 0.3	V
Interface signal (Logic "L")	V_{IL}	−0.3	V
Supply voltage (Logic)	V_L	+7	V
Supply voltage (Panel drive)	V_D	+14	V
Operating temperature	Topr	−5 to +55*1	°C
Storage temperature	Tstg	−40 to +80	°C

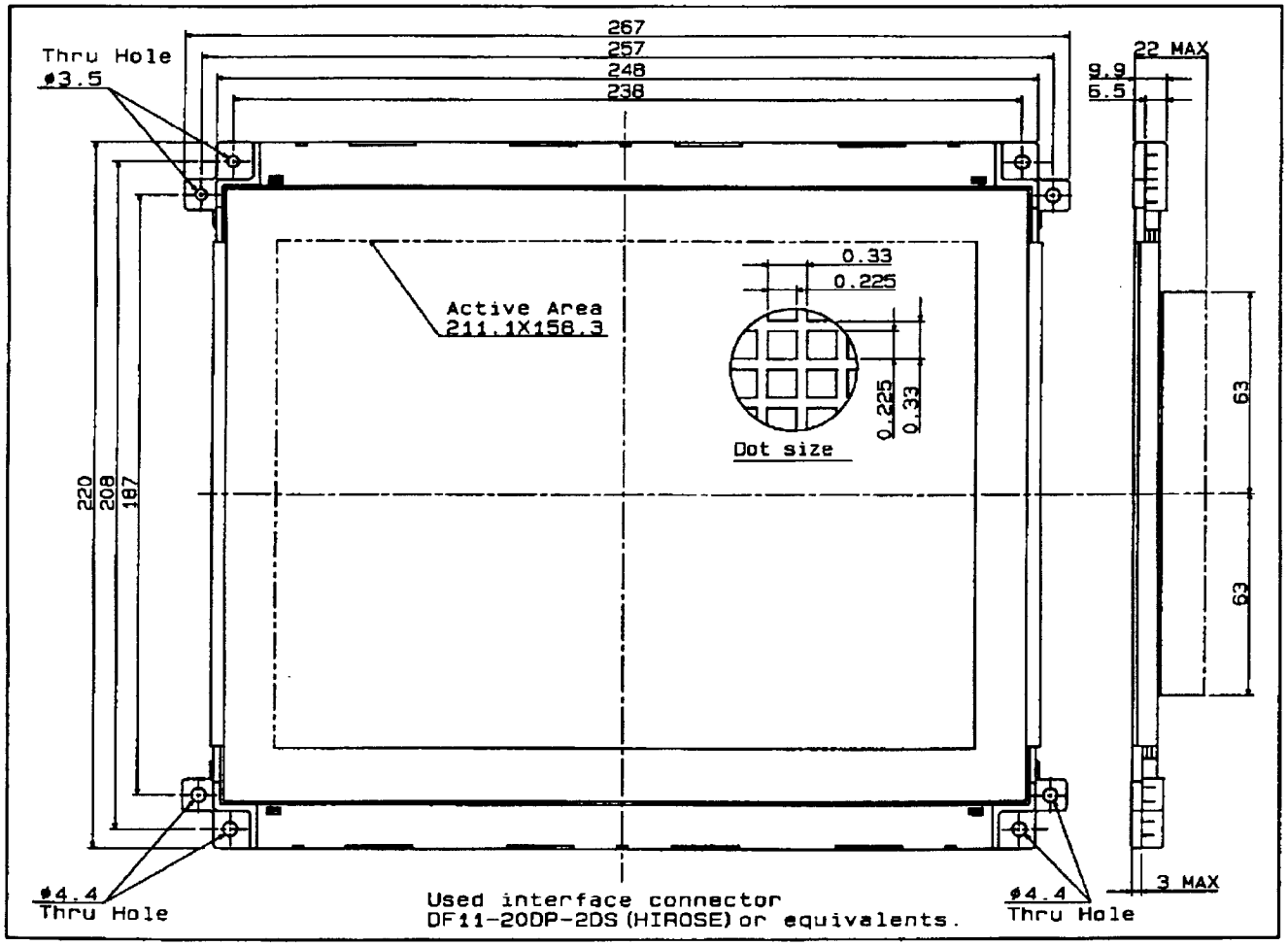
Note) • No dew condition
• *1 Survival Temperature Range:
(Operating)
Topr = −20 to +85 °C
Although there is a possibility of visible noise or unevenness on the panel, permanent damage shall not be sustained.
(No condensation)

■ Corresponding connector for interface

DF11-20DS-2C (HIROSE) or equivalents
(crimp contact: DF11-2428SC)

Outline Dimensions

(Unit:mm)



Electro-optical Characteristics

(Ta=25 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5 V	30	—	300	mA
Supply voltage (Panel drive)	V_D	—	11.4	12.0	12.6	V
Supply current (Panel drive)	I_D	V_D=12 V	(*1)	—	1 500	mA
Power consumption	P_T	V_L=5 V, V_D=12 V	—	12	—	W
Luminance	L_{ON}	All dots lit	137	200	—	cd/m²
Off luminance	L_{OFF}	All dots turned off	—	—	3.4	cd/m²
Luminance distribution	ΔL_{DIS}	All dots lit	—	—	35	%
Fill factor			—	0.46	—	
Shadowing characteristics	ΔL_{SD}	Fixed pattern	—	2	—	%
Viewing angle			—	160	—	°

(*1) 10 mA in condition with no signals nor V_L supplying

Interface Timing Ratings

(Ta=25 °C)

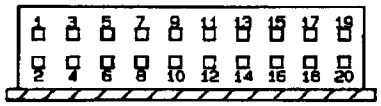
Parameter	Symbol	Min.	Typ.	Max.	Unit
Frame frequency	$1/T_{FRM}$	60	—	120	Hz
CP2 clock cycle	T_{CP2}	154	—	—	ns
High level clock width	t_{CWH}	60	—	—	ns
Low level clock width	t_{CWL}	60	—	—	ns
CP1 clock cycle	t_{CP1}	31	—	—	µs
High level latch clock width	t_{LWH}	60	—	—	ns
Data set up time	t_{SU}	50	—	—	ns
Data hold time	t_H	40	—	—	ns
CP1 ↑ clock allowance time from CP2 ↓	t_{SZ1}	0	—	—	ns
CP2 ↓ clock allowance time from CP1 ↓	t_{S12}	200	—	—	ns
Clock rise/fall time	t_r, t_f	—	—	t_r*	ns

* $t_r = (T_{CP2} - t_{CWH} - t_{CWL})/2 \leq 30$ ns max.

Interface Signals

Pin No.	Symbol	Description
1	UD1	Display data signal (for the upper part of display)
2	UD0	
3	UD3	
4	UD2	
5	LD1	Display data signal (for the lower part of display)
6	LD0	
7	LD3	
8	LD2	
9	CP2	Data input clock signal
10	GND	Ground
11	CP1	Input data latch signal
12	GND	Ground
13	S	Scan start-up signal
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	V_L	+5 V
18	V_L	+5 V
19	V_D	+12 V
20	V_D	+12 V

Connector



Interface Timing Chart